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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,221	GOSIOR ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 09/843,178. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claim 1 of the instant application contains every element of claim(s) 1 of the copending Application No. 09/843,178 and as such anticipate(s) claim(s) 1 of the copending Application No. 09/843,178.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because in Fig. 1, reference character "38" has been used to designate both "ROM" and "External Devices, Memory, Processors, DSPs". Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended.

The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 2-4, 6, and 7 are objected to because of the following informalities:

In claim 2, line 1, it is suggested to change "A system" to -The system- since it was mentioned in claim 1 previously. Similar problems also exist in claims 3-18.

Claim 4, lines 1-2, "said processor logic and system memory" lacks proper antecedent basis since it was not mentioned in the previous claims. It is suggested to change "said processor logic and system memory" to - said logic mechanism and said at least one memory -.

In claim 6, line 2, "the internal clock rate" lacks proper antecedent basis since it was not mentioned in the previous claims. It is suggested to change "the internal clock rate" to - the internal clock frequency -.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 15-16, it is not clear how at least one memory can execute the instruction set data since the main function of a memory is to store data.

In claim 3, "a minimal number in a logic chain" is indefinite since where the logic chain is located in the system and how to determine the minimal number for the logic chain were not well defined.

In claim 5, lines 2-3, it is not clear what is meant by "connecting an internal clock to an external crystal frequency" since a frequency is not a hardware which can not be connected with a clock.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1 and 4 are rejected under 35 U.S.C. 102(a) as being anticipated by Borkenhagen et al. (U.S. Patent No. 6,076,157) (hereafter referred to as Borkenhagen et al.'157).

Referring to claim 1, Borkenhagen et al. discloses, as claimed, a programmable, low gate latency, system-on-chip embedded processor system for supporting general input/output applications, comprising: a modular, multiple bit, multithread processor core (260, 270, or 280, see Fig. 3) operable by at least four parallel and independent application threads (note n branch unit 260, n floating point unit 270, and n floating point unit 280 as shown in Fig. 3 together are *operable* by at least four parallel and independent application threads) sharing

common execution logic segmented into a multiple stage processor pipeline (see Col. 7, lines 16-20, regarding the Hinton et al.'855's processor core can be a single integrated circuit, pipelined, superscalar microprocessor), wherein said processor core is capable of having at least two states (best reasonably and broadly interpreted such as "wait", "ready", and running" states of the processor cores 260, 270, or 280); a logic mechanism (thread switch logic 400, se Fig. 2) engaged with said processor core (260, 270, or 280, see Fig. 3) for executing an instruction set within said processor core (260, 270, or 280, see Fig. 3) to generate instruction state (such as read and write state due to I/O operation codes in the instruction) data; a supervisory control unit (storage control unit 200, see Fig. 2), controlled by at least one of said processor core threads (such as the thread comprising the code for I/O operations, read or write to memories), for examining said core processor state and for controlling said core processor operation (as set forth, such as the thread comprising the code for I/O operations, read or write to memories); at least one memory (Main Memory 140 or L1 I-Cache 150, see Fig. 3, control stack or flag registers existing in the Hinton et al.'855's system) for storing and executing said instruction set data and for storing system values (flags or control bits in the Hinton et al.'855's

system); and a peripheral adaptor (Bus Interface 152, see Fig. 1) engaged with said processor core (260, 270, or 280, see Fig. 3) for transmitting input/output signals to and from said processor core.

As to claim 4, Hinton et al.'855 also discloses: the processor logic and system memory (Main Memory 140 or L1 I-Cache 150, see Fig. 3) are constructed from substantially the same integrated circuit process technology (see Col. 7, lines 16-20, regarding the Hinton et al.'855's processor core 100 can be a single integrated circuit, pipelined, superscalar microprocessor).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 3, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al.'855 in view of Douglas et al. (U.S. Patent No. 6,609,193) hereafter referred to as Douglas et al.'193).

Hinton et al.'855 discloses the claimed invention except for: stages of said pipeline are capable of breaking each instruction decode operation into multiple sub-processing steps within a logic chain (in clam 2); any of the processor threads can be disabled by said processor core to conserve power(claim 16); and the supervisory control unit is capable of changing the core processor operation to provide power management function (claim 18).

Douglas et al.'193 discloses a system for multi-thread pipelined instruction decoder comprising: stages of said pipeline are capable of breaking each instruction decode operation into multiple sub-processing steps (see Fig. 6, pipestages PS1, PS2, …, PSM of the instruction decode pipeline) within a logic chain (see Fig. 4, and Col. 9, lines 40-47, regarding "the illustrations provided in FIGS. 8-10, 11A and 11B are associated with the control of the instruction decode pipeline 400' between buffer 502A and buffer 502B in FIG. 5. Pipestages 513 through 517 are referred to as pipestages PS1

through PS5 but can be generalized to the control of any instruction decode pipeline within an instruction decoder"); any of the processor threads can be disabled by said processor core (power down logic 603 in Fig. 6, see also col. 8, lines 57-59, regarding "The power down logic 603 illustrated in FIG. 6, executes the "Powerdown for any PipeStage X" equation for each pipestage") to conserve power; and the supervisory control unit is capable of changing the core processor operation to provide power management function (as set forth, see also col. 8, lines 57-59, regarding "The power down logic 603 illustrated in FIG. 6, executes the "Powerdown for any PipeStage X" equation for each pipestage", the power down logic 603 provides the management function).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Hinton et al.'855's system to comprise stages of said pipeline are capable of breaking each instruction decode operation into multiple sub-processing steps within a logic chain, as taught by Hinton et al.'855, in order to facilitate gradually controlling the progress of each decoding process; and to modify Hinton et al.'855's system to comprise any of the processor threads can be disabled by said processor core to conserve power; and the supervisory control unit is capable of changing the core

processor operation to provide power management function, as taught by Hinton et al.'855, in order to save the power consumption for the Hinton et al.'855's system

Regarding claim 3, Hinton et al.'855 discloses, as best understood, a minimal number of gates in a logic chain to reduce the effects of gate latency (see the gates used in the storage control unit 200 as shown in Fig. 3).

Allowable Subject Matter

10. Claims 5-15 and 17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure wherein Kalafatis et al.'905, discloses a method and apparatus for thread switching within a multithreaded processor comprising a decoder 112 and the utilization of processor resources is distributed between threads according to the quantity of instruction data

for a particular thread that has been processed; and Emer et al.'443 discloses a pipelined multi-thread processor selecting thread instruction in inter-stage buffer based on count information. A selection logic circuit has an output coupled to the buffer to determine which instruction is to be read from the buffer based on the count information stored by the count logic. In operation, a thread may be selected for execution based on a selected attribute to enhance processing performance.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

13. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
June 16, 2004